Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (currently amended). A method for dynamically configuring a redundant area of a page associated with a physical block of a non-volatile memory of a memory system, the method comprising:

determining ~~when~~ whether at least one byte associated with the redundant area is to be altered, the at least one byte including error correction code (ECC) information associated with a first ECC algorithm; and

altering the at least one byte ~~when it is determined~~ responsive to determining that the at least one byte is to be altered, wherein altering the at least one byte includes altering the at least one byte to include ECC information associated with a second ECC algorithm.

2 (original). The method of claim 1 wherein the first ECC algorithm is a 1-bit ECC algorithm.

3 (currently amended). The method of claim 2, wherein ~~when~~ the at least one byte includes ECC information associated with the first ECC algorithm, ~~the at least one byte~~ and includes:

approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page,

approximately three bytes arranged to be used to correct an error associated with a second group of bytes of the data area, and

approximately two bytes arranged to be used to correct an error associated with the redundant area.

4 (original). The method of claim 2 wherein the second ECC algorithm is a 2-symbol ECC algorithm.

5 (currently amended). The method of claim 4 wherein ~~when~~ the at least one byte includes ECC information associated with the second ECC algorithm, ~~the at least one byte~~ and includes:

approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and

approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

6 (currently amended). The method of claim 1 further including:

obtaining at least one bit which is arranged to indicate a number of times the physical block has been erased from the redundant area, wherein determining ~~when~~ whether the at least one byte is to be altered includes determining ~~when~~ whether the at least one bit is approximately equal to a predetermined value.

7 (original). The method of claim 1 wherein the at least one bit includes information associated with an erase count of the physical block.

8 (currently amended). The method of claim 1 wherein the at least one byte associated with the redundant area is to be altered includes determining ~~when~~ whether a number of erase cycles undergone by the physical block has reached a threshold level.

9 (original). The method of claim 1 wherein altering the at least one byte includes storing the at least one byte which includes ECC information associated with the second ECC algorithm in the redundant area.

10 (original). The method of claim 1 wherein the non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

11 (currently amended). A memory system comprising:

a non-volatile memory, the non-volatile memory including a physical block, wherein the physical block has a page with a data area and a redundant area;

code devices that cause a determination to be made as to ~~when~~ whether at least one byte associated with the redundant area is to be altered, the at least one byte including error correction code (ECC) information associated with a first ECC algorithm;

code devices that cause the at least one byte to be altered ~~when it is determined~~ responsive to determining that the at least one byte is to be altered, wherein the code devices that cause the at least one byte to be altered include code devices that cause the at least one byte to be altered include ECC information associated with a second ECC algorithm; and

a memory section that stores the code devices.

12 (original). The memory system of claim 11 wherein the first ECC algorithm is a 1-bit ECC algorithm.

13 (currently amended). The memory system of claim 12 wherein ~~when~~ the at least one byte includes ECC information associated with the first ECC algorithm, ~~the at least one byte~~ and includes:

approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page,

approximately three bytes arranged to be used to correct an error associated with a second group of bytes of the data area, and

approximately two bytes arranged to be used to correct an error associated with the redundant area.

14 (original). The memory system of claim 12 wherein the second ECC algorithm is a 2-symbol ECC algorithm.

15 (currently amended). The memory system of claim 14 wherein ~~when~~ the at least one byte includes ECC information associated with the second ECC algorithm, ~~the at least one byte~~ and includes:

approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and

approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

16 (currently amended). The memory system of claim 11 further including:

code devices that cause at least one bit ~~which is~~ arranged to indicate a number of times the physical block has been erased to be obtained from the redundant area, wherein the code devices that cause a determination to be made as to ~~when~~ whether the at least one byte is to be altered include code devices that cause a determination to be made as to ~~when~~ whether the at least one bit is approximately equal to a predetermined value.

17 (original). The memory system of claim 11 wherein the at least one bit includes information associated with an erase count of the physical block.

18 (currently amended). The memory system of claim 11 wherein the code devices that cause a determination to be made as to ~~when~~ whether the at least one byte associated with the redundant area is to be altered currently amended code devices that cause a determination to be made as to ~~when~~ whether a number of erase cycles undergone by the physical block has reached a threshold level.

19 (original). The memory system of claim 11 wherein the code devices that cause the at least one byte to be altered include code devices that cause the at last one byte which includes ECC information associated with the second ECC algorithm to be stored in the redundant area.

20 (original). The memory system of claim 11 wherein the non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

21 (currently amended). A memory system comprising:

a non-volatile memory, the non-volatile memory including a physical block, wherein the physical block has a page with a data area and a redundant area;

means for determining ~~when~~ whether at least one byte associated with the redundant area is to be altered, the at least one byte including error correction code (ECC) information associated with a first ECC algorithm;

means for altering the at least one byte ~~when it is determined~~ responsive to determining that the at least one byte is to be altered, wherein altering the at least one byte includes altering the at least one byte to include ECC information associated with a second ECC algorithm.

22 (currently amended). The memory system of claim 21 wherein the first ECC algorithm is a 1-bit ECC algorithm and wherein ~~when~~ the at least one byte includes ECC information associated with the first ECC algorithm~~, the at least one byte~~ and includes:

approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page,

approximately three bytes arranged to be used to correct an error associated with a second group of bytes of the data area, and

approximately two bytes arranged to be used to correct an error associated with the redundant area.

23 (currently amended). The memory system of claim 22 wherein the second ECC algorithm is a 2-symbol ECC algorithm, and wherein ~~when~~ the at least one byte includes ECC information associated with the second ECC algorithm, ~~the at least one byte~~ and includes:

approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and

approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

24 (currently amended). The memory system of claim 21 further including:

means for obtaining at least one bit which is arranged to indicate a number of times the physical block has been erased from the redundant area, wherein the means for determining ~~when~~ whether the at least one byte is to be altered include means for determining ~~when~~ whether the at least one bit is approximately equal to a predetermined value.

25 (original). The memory system of claim 21 wherein the at least one bit includes information associated with an erase count of the physical block.

26 (original). The memory system of claim 21 wherein the non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

27 (currently amended). A method for processing a page associated with a physical block of a non-volatile memory of a memory system, the method comprising:

determining ~~when~~ whether at least one byte associated with a first error correction code (ECC) algorithm is to be altered to be associated with a second ECC algorithm, the at least one byte being stored in a redundant area associated with the page; and

dynamically configuring the redundant area ~~when it is determined~~ responsive to determining that the at least one byte is to be altered such that the at least one byte is altered to be associated with the second ECC algorithm.

28 (original). The method of claim 27 wherein the first ECC algorithm is a 1-bit ECC algorithm and the second ECC algorithm is a 2-symbol ECC algorithm.

29 (currently amended). The method of claim 28 wherein ~~when~~ the at least one byte associated with the first ECC algorithm includes:

approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page,

approximately three bytes arranged to be used to correct an error associated with a second group of bytes of the data area, and

approximately two bytes arranged to be used to correct an error associated with the redundant area.

30 (currently amended). The method of claim 28 wherein ~~when~~ the at least one byte is altered to be associated with the second ECC algorithm, ~~the at least one byte~~ and includes:

approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and

approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

31 (currently amended). The method of claim 27 wherein determining ~~when~~ whether the at least one byte is to be altered includes determining ~~when~~ whether an indicator stored in the redundant area indicates that the at least one byte is to be altered.

32 (currently amended). The method of claim 31 wherein the indicator is arranged to indicate a number of times the physical block has been erased, and wherein ~~when~~ whether the indicator is approximately equal to a predetermined value, the indicator indicates that the at least one byte is to be altered.

33 (currently amended). A method for dynamically configuring a redundant area of a page associated with a physical block of a non-volatile memory of a memory system, the method comprising:

determining ~~when~~ whether a set of bits in the redundant area is to be altered, the bits including error correction code (ECC) information associated with a first ECC algorithm, wherein the set of bits are substantially grouped in a first configuration; and

altering the set of bits ~~when it is determined~~ responsive to determining that the set of bits is to be altered, wherein altering the set of bits includes altering the set of bits to include ECC information associated with a second ECC algorithm and grouping the set of bits in a second configuration.

34 (original). The method of claim 33 wherein the set of bits includes approximately eight bytes and the first configuration includes a first subset of approximately three bytes, a second subset of approximately three bytes, and a third subset of approximately two bytes.

35 (original). The method of claim 34 wherein the second configuration includes a first grouping of approximately five bytes and a second grouping of approximately three bytes.

36 (original). The method of claim 33 wherein the first ECC algorithm is a 1-bit ECC algorithm and the second ECC algorithm is a 2-symbol ECC algorithm.

37 (currently amended). The method of claim 33 wherein determining ~~when~~ whether the set of bits is to be altered includes determining ~~when~~ whether an indicator stored in the redundant area indicates that the set of bits is to be altered.

38 (currently amended). The method of claim 37 wherein the indicator is arranged to indicate a number of times the physical block has been erased, and wherein ~~when the indicator is approximately equal to a predetermined value,~~ the indicator indicates that the set of bits is to be altered by having a value approximately equal to a predetermined value.